1. Apparatus for reducing quantization error in an analog computation for converting an input representing force to an analog force output representing force in terms of a force actuator signal to be input to a force actuator, wherein the input representing force is based on an input resolution, the apparatus comprising:

a processor programmed to convert the input to two analog force signals and a plurality of digital logic signals, the analog force signals representing an analog upper end and an analog lower end of a range of the force actuator signal, the range including the value of the force actuator signal, the digital logic signals having a resolution less than or equal to 12 bits and being equal to the input resolution, the digital logic signals representing the force actuator signal in the range;

a difference circuit for generating an analog range voltage signal representing the range of the force actuator signal;

a divider circuit for dividing the analog range voltage signal by the resolution of the digital logic signals to output an analog force increment signal in terms of voltage;

first analog circuitry responsive to logic defined by the digital logic signals for converting the analog force increment signal to an analog force set point signal; and

second analog circuitry for adding one of the analog force signals to the analog force set point signal to determine the value of the force actuator signal.

2. Apparatus as recited in claim 1, wherein the first analog circuitry comprises:

digital logic circuitry responsive to logic of the digital logic signals for selecting an analog logical voltage signal; and

analog multiplier circuitry for multiplying the analog force increment signal by the analog logical voltage signal to output a voltage value of the analog force set point signal.

3. Apparatus as recited in claim 1, wherein the first analog circuitry comprises:

logic evaluation circuitry having one logic input corresponding to each bit of the resolution of the digital logic signals, the logic evaluation circuitry having one binary logical output corresponding to each count of the resolution of the digital logic signals;

logic multiplier circuitry comprising one multiplier corresponding to each count of the resolution of the digital logic signals, each multiplier having one binary logical input corresponding to each binary logical output, the multipliers having one logic voltage input having different values selected according to the number of counts of the resolution of the digital logic signals, each multiplier having a set point factor output;

a series of adder circuits for respectively sequentially adding two of the set point factor outputs to produce a first sum, the adder circuits adding a next set point factor to the first sum to produce a next sum and adding in sequence until a final next sum is a sum having a number one less that the value of the count of the resolution; and

a multiplier circuit having the final next sum as a first input and the analog force increment signal as a second input, the multiplier outputting the analog force set point signal.

4. Apparatus for reducing quantization error in an analog computation for converting an input representing force in terms of units of force to an analog force output representing force in terms of a signal to be input to a force actuator, the apparatus comprising:

a processor programmed to convert the input to two analog force signals and a plurality of digital logic signals, the analog force signals representing the boundaries of a range of signals to be input to a force actuator, the range including a force actuator signal having a value corresponding to the value of the force in force units, each of the digital logic signals having a resolution less than or equal to 12 bits, the digital logic signals together representing the force actuator signals in the range having the value corresponding to the value of the force in force units;

first analog circuitry responsive to the resolution of the digital logic signals for converting a difference between the two analog force signals to an analog force increment signal;

second analog circuitry responsive to logic defined by the digital logic signals for converting the analog force increment signal to an analog force set point signal; and

third analog circuitry for adding one of the analog force signals to the analog force set point signal to determine the value of the force actuator signal.

5. Apparatus as recited in claim 4, wherein the input representing force in terms of units of force is based on an input resolution, and wherein the input resolution equals the resolution of the digital logic signals.

6. Apparatus as recited in claim 4, wherein the first analog circuitry comprises

a difference circuit for generating an analog range voltage signal representing the range of the force actuator signal, the range being the difference between the two analog force signals; and

a divider circuit for dividing the analog range voltage signal by a function of the resolution of the digital signals to output the analog force increment signal in terms of voltage.

7. Apparatus as recited in claim 4, wherein the second analog circuitry comprises:

digital logic circuitry responsive to logic of the digital logic signals for selecting an analog logical voltage signal; and

analog multiplier circuitry for multiplying the analog voltage force increment signal by the analog logical voltage signal to output a voltage value of the analog force set point signal.

8. Apparatus as recited in claim 4, wherein the second analog circuitry comprises:

logic evaluation circuitry having one logic input corresponding to each bit of the resolution of the digital logic signals, the logic evaluation circuitry having one binary logical output corresponding to each count of the resolution of the digital logic signals;

logic multiplier circuitry comprising one multiplier corresponding to each count of the resolution of the digital logic signals, each multiplier having one binary logical input corresponding to each binary logical output, the multipliers having one logic voltage input having different values selected according to the number of counts of the resolution of the digital logic signals, each multiplier having a set point factor output;

a series of adder circuits for respectively sequentially adding two of the set point factor outputs to produce a first sum, the adder circuits adding a next set point factor to the first sum to produce a next sum and adding in sequence until a final next sum is a sum having a number one less that the value of the count of the resolution; and

a multiplier circuit having the final next sum as a first input and the analog force increment signal as a second input, the multiplier outputting the analog force set point signal.

9. Apparatus for reducing quantization error in an analog computation for converting an input representing force in terms of units of force to an analog force output representing force in terms of a force actuator signal to be input to a force actuator, wherein the input representing force in terms of units of force is based on an input resolution; the apparatus comprising:

a processor programmed to convert the input to two analog force signals and a plurality of digital logic signals, the analog force signals representing the boundaries of a range of force actuator signals to be input to a force actuator, the range of the force actuator signals including the value of a force actuator signal having a value corresponding to the value of the force in force units; the digital logic signals having a resolution equal to the input resolution and less than or equal to 12 bits, the digital logic signals representing the force actuator signals in the range having the value corresponding to the value of the force in units of force;

a difference circuit for generating an analog range voltage signal representing the range of the force actuator signals, the range being the difference between the two analog force signals;

a divider circuit for dividing the analog range voltage signal by the resolution of the digital logic signals to output an analog force increment signal in terms of voltage;

first analog circuitry responsive to logic defined by the digital logic signals for converting the analog force increment signal to an analog force set point signal; and

second analog circuitry for adding one of the analog force signals to the analog force set point signal to determine the value of the force actuator signal.

10. Apparatus as recited in claim 9, wherein the first analog circuitry comprises:

digital logic circuitry responsive to logic of the digital logic signals for selecting an analog logical voltage signal; and

analog multiplier circuitry for multiplying the analog force increment signal by the analog logical voltage signal to output a voltage value of the analog force set point signal.

11. Apparatus as recited in claim 9, wherein the first analog circuitry comprises:

logic evaluation circuitry having one logic input corresponding to each bit of the resolution of the digital logic signals, the logic evaluation circuitry having one binary logical output corresponding to each count of the resolution of the digital logic signals;

logic multiplier circuitry comprising one multiplier corresponding to each count of the resolution of the digital logic signals, each multiplier having one binary logical input corresponding to each binary logical output, the multipliers having one logic voltage input having different values selected according to the number of counts of the resolution of the digital logic signals, each multiplier having a set point factor output;

a series of adder circuits for respectively sequentially adding two of the set point factor outputs to produce a first sum, the adder circuits adding a next set point factor to the first sum to produce a next sum and adding in sequence until a final next sum is a sum having a number one less that the value of the count of the resolution; and

a multiplier circuit having the final next sum as a first input and the analog force increment signal as a second input, the multiplier outputting the analog force set point signal.